(Translation)

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Notification of Reason(s) for Refusal

Patent Application No.	JP2002-563630
Drafting Date	July 13, 2005
Examiner of JPO	Noriyuki MAEDA
Representative / Applicant	M. Nakamura (and 8 others)
Applied Provision	Patent Law Sections 29(2) and 36

This application should be refused for the reasons mentioned below. If the applicant has any argument to make against this notification, such an argument should be submitted within 3 months from the date on which this notification was dispatched.

Reasons

Reason 1 This application does not comply with the requirements under Patent Law Sections 36(4) and 36(6)(i)(ii) regarding the descriptions of claims, specification and drawings for the reasons stated below.

Reason 2 The inventions in the Claims of this application stated below should not be granted a patent under the provision of Patent Law Section 29(2) since they could have easily been made by persons who have common knowledge in the technical field to which the inventions pertain, on the basis of the inventions described in the publications listed below which were distributed in Japan or foreign countries or the inventions made available to the public through electric telecommunication lines prior to the filing of this application.

Notes

No.1 With regard to Reason 1

1. It is unclear as to what and how do the inventions of claims 1 - 32 monitor with regard to an optoelectronic device.

2. inventions of claims 1 - 7

The inventions of claims 1 - 7 are not only indefinite with regard to the following points (1) - (5) but also not supported by Detailed Description of Invention.

(1) "memory" is unclear.

1) It is unclear as to what kind of information the "information related to the optoelectronic device" is.

(2) Regarding "a plurality of analog signals corresponding to operating conditions of the optoelectronic device", it is extremely unclear as to what kind of operating conditions they are, what kind of analog signals they are and how the analog signals correspond to the operating conditions.

1) "operating condition" is unclear as to what kind of operation it is for, and as to what kind of conditions they are.

2) It is unclear as to how the "a plurality of analog signals" correspond to the "operating conditions".

(3) "analog to digital conversion circuitry" is unclear.

1) "predefined locations within the memory" is unclear.

(4) "comparison logic" is unclear as to what it is like.

1) Definition of the "limit values" is unclear.

2) The relationship is unclear between "to compare the digital values with limit values" and "to generate flag values".

3) It is unclear as to what kind of "storage locations" the "predefined flag storage locations" are like.

(5) It is unclear how "an interface" is configured.

1) It is unclear as to what kind of "storage locations" the "predefined flag storage locations" are like.

2) It is unclear as to how "a flag value" is defined.

3. inventions of claims 2 - 5 and 7

It is unclear as to how the locations of "a power level location", "a power flag location", "a temperature location" and "a temperature flag location" are defined and as to how they are used. Further, it is also unclear how the information stored is utilized.

4. invention of claim 8

The invention of claim 8 is not only indefinite with regard to the following points (1) - (5) but also not supported by Detailed Description of Invention.

(1) The definition of "memory" is unclear.

It is unclear as to what kind of information the "information related to the optoelectronic device" is and as to how it relates to the optoelectronic device.

(2) "analog to digital conversion circuitry" is unclear.

1) Although "laser bias current", "laser output power" and "received power" are set forth regarding "a plurality of analog signals corresponding to operating conditions of the optoelectronic device", it is unclear as to how these analog signals correspond to the operating conditions of the optoelectronic device.

2) It is unclear as to how "predefined locations within the memory" are defined.

(3) It is unclear as to what kind of logic "comparison logic" is.

1) The definition of "limit values" is unclear.

2) The relationship is unclear between comparing digital values with the limit values and generating a flag value.

3) It is unclear as to what king of storage locations "predefined flag storage locations" is.

(4) It is unclear as to how "an interface" is configured.

1) It is unclear as to what king of storage locations "predefined flag storage locations" is.

2) It is unclear as to how "flag values" are defined.

5. inventions of claims 10 - 13 and 15

It is unclear as to how the locations of "a power level location", "a power level flag location", "a temperature location" and "a temperature flag location" are defined and as to how they are used. Further, it is also unclear how the information stored is utilized.

6. inventions of claims 9 - 15, 17 - 23 and 24

The inventions of claims 9 - 15, 17 - 23 and 24 are not only indefinite with regard to the following points (1) - (5) but also not supported by Detailed Description of Invention.

(1) "A plurality of analog signals corresponding to operating conditions of the

optoelectronic device" is extremely unclear.

1) "operating condition" is unclear as to what kind of operation it is for, and as to what kind of conditions they are.

2) It is unclear as to how the "a plurality of analog signals" correspond to the "operating conditions".

(2) The third paragraph of claim 9 is unclear with regard to the following points.

1) The definition of "limit values" is unclear.

2) The relationship is unclear between comparing digital values with the limit values and generating a flag value.

3) It is unclear as to what king of storage locations "predefined flag storage locations" and "predefined memory-mapped flag storage locations" are.

(3) The fourth paragraph of claim 9 is unclear with regard to the following point.

1) It is unclear as to what kind of locations "host-specified locations within the memory, including the predefined flag locations" and "host-specified memory-mapped locations within the optoelectronic device, including the predefined memory-mapped flag storage locations" are.

7. inventions of claims 18 - 23

It is unclear as to how the locations of "a memory-mapped power level location", "a memory-mapped power level flag location", "a memory-mapped temperature location" and "a memory-mapped temperature flag location" are defined and as to how they are used. Further, it is also unclear how the information stored is utilized.

8. invention of claim 24

The invention of claim 24 are not only indefinite with regard to the following points (1) - (5) but also not supported by Detailed Description of Invention.

(1) It is unclear as to how "an interface" is configured.

1) It is unclear as to what king of storage locations "a predefined memory-mapped flag storage locations" is.

2) It is unclear as to how "flag values" are defined.

(2) Although "laser bias current", "laser output power" and "received power"

are set forth regarding "a plurality of analog signals corresponding to operating conditions of the optoelectronic device", it is unclear as to how these analog signals correspond to the operating conditions of the optoelectronic device.

9. inventions of claims 25 - 31 and 32

The inventions of claims 25 - 31 and 32 are not only indefinite with regard to the following points (1) - (5) but also not supported by Detailed Description of Invention.

(1) "storing the digital values in predefined memory-mapped locations" is unclear.

1) "operating condition" is unclear as to what kind of operation it is for, and as to what kind of conditions they are.

2) It is unclear as to how the "a plurality of analog signals" correspond to the "operating conditions". Although "laser bias current", "laser output power" and "received power" are set forth, it is unclear as to how these analog signals correspond to the operating conditions of the optoelectronic device.

(2) "storing the flag values in predefined memory-mapped flag locations" is unclear.

1) The definition of "limit values" is unclear.

2) The relationship is unclear between comparing digital values with the limit values and generating a flag value.

3) It is unclear as to what king of storage locations "predefined flag storage locations" and "predefined memory-mapped flag storage locations" are.

(3) "enabling the host device to read from host-specified memory-mapped locations within the optoelectronic device, including the predefined memory-mapped flag locations" is unclear.

10. summary

As mentioned above, the inventions of claims 1 - 32 are extremely unclear, and thus these inventions can not be clearly understood, nor implemented. Accordingly, the examination of the requirements for patentability, such as novelty, an inventive step and so on, regarding the present application can not be properly conducted.

No.2 With regard to Reason 2

(1) list of cited document

cited document 1: JP09-162811A

(2) comparison and study

Since the inventions of claims 1 - 32 are extremely unclear, novelty and an inventive step with regard to these inventions can not be examined properly. However, the following document can be cited as a related document.

There is a following description in cited document 1 along with the drawings.

"[0022]

[Detailed Description of the Invention]

<Optical Transmission Apparatus> A block diagram of an example of the present invention is set forth in Fig. 1. An optical transmission apparatus 1 comprises an optical transmitter 2 and optical receiver 3 on a circuit substrate.

...(omission)...

[0024] The optical transmitter 2 and the optical receiver 3 share a microcomputer 4 which is composed of a semiconductor integrated circuit. The microcomputer 4 is a circuit module which generally controls optical transmission apparatus 1, for example, it may be able to detect a temperature characteristic of LD200, use a data table which is made based on the detected temperature characteristic, control a driving current based on the temperature characteristic of LD200 according to an optical output, temperature and so on which LD module 20 requires, or control a dynamic range of signals received at a preamplifier 31. That is, the microcomputer 4 is an example of a data processing device which controls a semiconductor device according to a characteristic information of the semiconductor device previously measured. In addition, the microcomputer 4 can interface with the outside of the optical transmission device 1.

...(omission)...

[0026] <Optical Transmitter> A detailed example of said optical transmitter 2 is depicted in Fig. 3.

...(omission)...

[0033] The microcomputer 4 has a central processing unit (CPU) 41, a RAM 42,

ROMs 43, 49 and a timer (TMR) 48, each of which is connected to an inner bus 40, and it has interface means which are analog input circuit 44, analog output circuit 45 and the other I/O circuit 46 which are connected to the inner bus, and further it has a watchdog timer 47 for detecting a runaway and the like. These circuit modules are formed on a single integrated semiconductor substrate. Said RAM 42 may be a waking area or a temporary storage area for data. As said ROM 43, an electrically writable non-volatile semiconductor storage device, such as an electrically rewritable flash memory, an EEPROM (electrically erasable and programmable read-only memory) or electrically writable and ultra violet erasable EPROM (electrically programmable read-only memory) can be adopted. Said ROM 43 is used for storing an operation program of CPU41 and it can be constituted by a rewritable mask ROM. Or else, the program and data can be stored in a single ROM. In that case, the ROM must be constituted by an electrically writable ROM.

[0034] The analog input circuit 44 comprises, for example, four analog-to-digital converters A/D1 - A/D4 and four latch circuits LAT1 - LAT4 which latch respective output data from the analog-to-digital converters A/D1 - A/D4 and output to inner bus 40. Each of the analog-to-digital converters A/D1 - A/D4 has, for example, 8-bit conversion accuracy. Said analog output circuit 45 comprises, for example, two digital-to-analog converters D/A1 and D/A2, latch circuits LAT5 and LAT6 which receive two digital signals for respective digital-to-analog converters D/A1 and D/A2 from inner bus 40, and two band-pass filter BPF1 and BPF2 which reshape respective analog signals output from the digital-to-analog converters D/A1 and D/A2. The digital-to-analog converters D/A1 and D/A2 convert 8-bit digital signal into analog signal in 256 steps of gradation. Latch circuits LAT1 - LAT6 are laid out in an address space of CPU 41 and are configured to be accessed by CPU 41. The microcomputer 4 has an operation mode by which it can directly access to the inner circuits, such as latch circuits LAT1 - LAT6, from outside through outer I/O circuit 46.

...(omission)...

[0037] By such an constituent feature mentioned above, CPU 41 can control a modulating current and a bias current flowing through LD200 respectively and arbitrarily in accordance with a digital data which is set in the latch circuits LAT5 and LAT6. Therefore, LD200 can be optically driven without any extinction error or light-emitting delay, by allowing CPU 41 to set data in the latch circuits LAT5

and LAT6, the data being adjusted to a temperature characteristic of LD200 under specific operating condition of the optical transmitting device 1, in other words, by setting data corresponding to a threshold current of LD200 at a temperature of operating atmosphere at that time in the latch circuit LAT5 and setting data corresponding to the modulating current which is to be added to said threshold current in the latch circuit LAT6 in order to obtain a required optical output under that temperature.

...(omission)...

[0046] The data which is obtained in a way mentioned above are written by the host device in a predetermined area of a table (the temperature characteristic table) in ROM 4 of the microcomputer 4. Such written data is the characteristic information for a laser diode. The table has the following structure (not illustrated). The first structure of the table has an information of said If(T) and Ith(T), for each temperature, which are correlated with a targeted optical output. In the situation where an LD is actually driven, CPU 41 selects If(T) and Ith(T) in accordance with the targeted optical output and the temperature, calculates If(T) - Ith(T), samples the values of LAT1 and LAT2, and then sets data in the latch circuit LAT5 so that the output value of the latch circuit LAT1 is equal to Ith(T) and sets data in the latch circuit LAT6 so that the output value of the latch circuit LAT2 is equal to If(T) - Ith(T).

[0047]

The second table structure calculates, in advance, If(T) - Ith(T) which are correlated with a targeted optical output for each temperature and has an information of If(T) - Ith(T) and If(T). In this case, when an LD is actually driven, CPU 41 selects If(T) - Ith(T) and Ith(T) in accordance with the targeted optical output and the temperature, samples the values of LAT1 and LAT2, and then sets data in the latch circuit LAT5 so that the output value of the latch circuit LAT1 is equal to Ith(T) and sets data in the latch circuit LAT6 so that the output value of the latch circuit LAT2 is equal to If(T) - Ith(T). In addition, the second table structure may have an information regarding If(T).

[0048]

The third table structure calculates, in advance, If(T) - Ith(T) which are correlated with a targeted optical output for each temperature, obtains setting data for the latch circuit LAT5 necessary for the output value of the latch circuit LAT1 to be Ith(T) and setting data for the latch circuit LAT6 necessary for the

output value of the latch circuit LAT2 to be If(T) - Ith(T), and has information which are to be set in said latch circuits LAT5 and LAT6 which are correlated with a targeted optical output for each temperature. In this case, when the an LD is actually driven, CPU 41 sets selected characteristic information in the latch circuits LAT5 and LAT6 directly according to the targeted optical output and temperature. In addition, the third table structure may have the same information as those of the first and the second table structure.

...(omission)...

[0052] CPU 41 detects the actual modulating current through the latch circuit LAT2, detects the actual bias current through the latch circuit LAT1, and further, detects the actual optical output of LD200 through the latch circuit LAT3 at a every pause timing or at a predetermined time interval set by a timer. CPU 41 compares these detected values with targeted values and if these detected values are largely different from the targeted values, for example, if these differences excess more than 20 %, then an exception handling is executed. For example, if an light emission anomaly of LD200 (extreme decrease of emission output) is detected, then CPU 41 reports it to the outside by control signal 13. A controller for communication which receives this report can issue an error status information on a communication line, or stop communicating. If the bias current which flows through transistor Tr1 extremely decrease, then CPU 41 can report it to the outside by said control signal 14. Further, one can adopt a following alternative processing, that is, when CPU 41 detects a situation for a predetermined time period where an optical emission output decreases less than a predetermined value (20 % less than targeted value, for example), CPU 41 judges that LD200 suffers from a characteristic degradation and set data in the latch circuits LAT5 and LAT6 in order to largely increase the optical emission outputs compared to those which were already specified. It is also possible to update the temperature characteristic data table according to such degradation. For this end, it is necessary that ROM 34 be constituted by a non-volatile semiconductor memory device so that it can be electrically rewritten by CPU 41."

No particular difference is found between the inventions of present claims 1 - 32 and the invention described in cited document 1. Accordingly, the examiner considers that the inventions of present claims 1 - 32 could have easily been made by a person skilled in the art based on cited document 1.

If a new reason(s) for refusal is found, the applicant will be notified thereof.

Record of the result of prior art search

Technical field(s) to be searched IPC 7th edition
H04B10/00 - 10/28
H04J14/00 - 14/08

Prior art document(s)
JP06-504405A
JP06-209209A
International Publication 98/00943 pamphlet
International Publication 98/00893 pamphlet

This record is not a component(s) of the reason(s) for refusal.

If the applicant has any question regarding his notification of reason(s) for refusal, or if an interview with the examiner is desired, please contact the following:

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PATENT ABSTRACTS OF JAPAN

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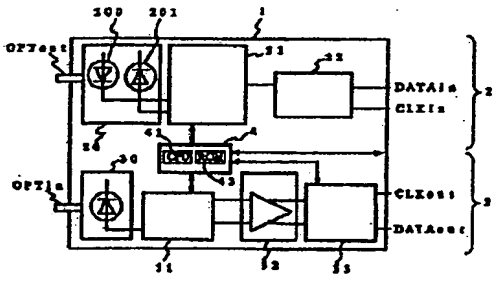
(54) CHARACTERISTIC INFORMATION GENERATING METHOD FOR SEMICONDUCTOR DEVICE MOUNT MODULE, OPTICAL TRANSMITTER AND LASER DIODE, AND OPTICAL TRANSMITTER

(57) Abstract:

PROBLEM TO BE SOLVED: To resolve defective extinction and delay in light emission due to difference between a temperature characteristic of a laser diode and a temperature characteristic of a circuit controlling the drive the laser diode.

SOLUTION: The optical transmitter 2 is provided with a nonvolatile storage means 43 storing characteristic information to decide a drive current of a laser diode 200 depending on a temperature and an object optical output. A control means 41 selects the characteristic information depending on the temperature and the object optical output from a nonvolatile storage means 43 to control a drive current supplied from a driver circuit 21 based thereon. Thus, the laser diode 200 is driven without extinction error and delay in light emission.



IMPORTANT NOTICE
REGARDING AMENDMENT AND DIVISIONAL

1. Amendment to the Claims

After a final office action issued, an amendment to the claims is strictly limited. Therefore, please keep in mind that the amendment to claim(s) in response to the present office action might be the last opportunity for the applicant to freely amend (broaden, add or change) claim(s) within the original disclosure. *(Detailed information is shown in the footnote.*)*

2. Divisional Application

Once the patent application is allowed, there is no opportunity to file a divisional application(s). Therefore, if you plan to file a divisional application(s) for any non-claimed subject matters, you should file such a divisional application(s) simultaneously with the response to the present office action.

** Footnote*

If the reason for refusal is not overcome by the response to the present office action, the examiner may issue a final office action (a "Final Notice of Rejection" or an "Decision for Final Rejection").

The "Final Notice of Rejection" is an office action issued during the examination procedure and therefore, the applicant can file an amendment in response thereto.

On the other hand, the "Decision for Final Rejection" is an office action issued at the end of the examination procedure and therefore, the applicant can not file an amendment in response thereto. To keep the application alive, an appeal must be filed. If the appeal is filed before the Trial Board of the Patent Office, the applicant can file an amendment within a 30-day period from the filing of the appeal.

In this connection, it should be noted that the scope of the amendment filed in response to the "Final Notice of Rejection" or filed within the 30-day period from the filing of the appeal is strictly limited to the following:

(a) Cancellation of a claim(s)
(b) Limitation of an element already recited in the claim(s) before the amendment
(c) Correction of errors, or
(d) Clarification of an unclear description.